

### REMARKS

Claims 1-22 were pending in the subject case. In the Office Action dated 10/24/02 ("Office Action"), Claims 1, 11, and 19 were rejected, and Claims 2-10, 12-18, and 20-22 were objected to. Claims 1-22 remain pending as previously presented. In view of the arguments set forth below, it is respectfully submitted the Claims are in condition for allowance.

### ARGUMENTS

1. Claims 1, 11, and 19 were rejected under 35 USC §102(b) as being anticipated by U.S. Patent No. 6,338,133 to Schroter ("Schroter"). This rejection is respectfully traversed.

Turning first to Claim 1, this Claim describes a first storage device to store a programmable count value indicative of a predetermined number of instructions, and a logic sequencer *to initiate concurrent execution* on the predetermined number of the instructions in a predetermined period of time within an instruction pipeline of an instruction processor. (Claim 1 lines 7-12.) This Claim describes the aspect of Applicants' invention wherein a predetermined programmable value is used to control the number of instructions that will begin concurrent execution within the pipeline.

The Examiner asserts that the aspects of Applicants' Claim 1 are taught by Schroter. In particular, the Examiner equates the Schroter execution units with Applicants' pipeline, and further correlates the Schroter threshold level with Applicants' count value. (See Office Action, sentence bridging pages 2 and 3.) Applicants' Representative disagrees with this assessment for at least the following reasons:

a.) Schroter describes a system for branch dispatching of instructions in a data processor. In that system, dispatch unit 20 (Schroter Figures 2 and 4a) retrieves one or more instructions from instruction queue 19, and dispatches them to the appropriate ones of the execution units FXU 11, LSU 28, and FPU 30. (Schroter

column 6 lines 1-5.) The instruction is stored within a queue of the execution unit, as follows:

"Each execution unit has a corresponding queue which hold instructions ***pending*** execution." (Schroter column 3 lines 31-32, emphasis added.)

When an execution unit is ready to execute an instruction, it obtains the instruction from its queue. When instruction execution is complete, the data results are provided to a storage device.

According to the Schroter system, the dispatch unit 20 may not always dispatch an instruction immediately to a queue of an execution unit. In particular, if an instruction is determined to be a speculative branch instruction, and further if a threshold number of instructions are already ***queued and waiting*** to be executed by one or more of the execution units, the speculative branch instruction will not be transferred to a queue of an execution unit. Instead, the dispatch unit will wait until the number of queued instructions is reduced to fewer than the threshold number before the speculative branch instruction will be transferred to the execution unit queue. This threshold number of instructions is determined by respective threshold values that are associated with each of the queues of the execution units. In one embodiment, a speculative branch instruction will not be stored within any queue of any execution unit until the number of instructions awaiting execution within each queue is reduced below that queue's respective threshold value. (Schroter column 6, line 62 through column 7, line 1.) In another embodiment, a speculative branch instruction is not stored to the queue of a particular execution unit until the number of instructions awaiting execution by that execution unit drops below a respective threshold value. (Schroter column 7, line 44 – 57.)

In summary, Schroter teaches a system that includes means for dispatching speculative instructions based on the number of instructions ***queued*** to one or more of the execution units. To re-state, in some situations involving speculative instructions, Schroter controls how many instructions are ***awaiting*** execution by delaying the dispatch of the speculative instruction. It does not appear that controlling the number of instructions ***awaiting*** execution in any way affects the number of instructions actually being executed by the various execution units at a

given point in time. Therefore, Schroter **does not** teach or even suggest Applicants' system of Claim 1 for controlling the number of **instructions being concurrently executed** within a pipeline, as the Examiner so asserts. In fact, since the goal of Schroter system is to increase execution throughput as much as possible by avoiding the penalties associated with incorrectly predicted branches, there would be no reason for Schroter to control (or in any way limit) the number of instructions being concurrently executed within the pipeline in a predetermined period of time.

The foregoing distinction between the Schroter system and Applicants' invention of Claim 1 is summarized in Schroter as follows:

"In one illustrative embodiment of the invention, the logic tracks how many instructions **are queued up** for each of the execution units and, based on a threshold for each execution unit, decides whether or not to dispatch speculative paths." (Schroter column 8 lines 29-34, emphasis added.)

This aspect of controlling the number of instructions that are **waiting** for processing by the Schroter execution units is reiterated as follows:

"...a unit's threshold refers specifically to a number of instructions which are located within the unit's instruction queue **awaiting** execution." (Schroter column 8 lines 39-41, emphasis added.)

Another passage from Schroter describes this aspect as follows:

"These circuit components [shown in FIG. 4A]...enable speculative dispatching only when a number of instructions **waiting for execution** is less than a is [sic] predetermined threshold." (Schroter column 9 lines 13-19, emphasis added.)

These cited passages make clear that the threshold values described in Schroter control how many instructions are waiting to be executed. These threshold values do not in any way control the number of instructions being concurrently executed by the execution units as the Examiner asserts. In fact, as noted above, since the goal of Schroter system is to increase instruction execution throughput as much as possible, there is no motivation in Schroter to control (or in any way limit) the number of instructions being concurrently executed within a predetermined period of time.

Thus, the Schroter system does not anticipate, or even suggest, Applicants' invention of Claim 1. This rejection is therefore improper and should be withdrawn.

b.) In addition to the foregoing, Claim 1 describes a sequencer to control the number of instructions received, and concurrently executed by, the *instruction pipeline*. Applicants' Specification describes the instruction pipeline as including multiple pipeline stages such as instruction decode, address generation, and arithmetic processing. The timing and logic associated with these stages is shown in Applicants' Figures 5 and 7, respectively.

Like Applicants' Specification, Schroter describes various pipeline stages of the Schroter pipeline, which include fetch, decode/dispatch, execute, finish, and completion stages. The execution units perform the execution stage of the pipeline. (Column 5, lines 44-49 and column 7, lines 65 – column 8, line 1.) Thus, at most, it may be said Schroter teaches using a threshold value to control, in some cases, the number of instructions awaiting processing by a ***single pipeline stage***, wherein that stage is the execution stage. This is in contrast to Applicants' Claim 1 which describes a sequencer to cause the ***instruction pipeline*** (including all stages) to receive, and to initiate concurrent execution on, a predetermined number of instructions. For this additional reason, Claim 1 is not anticipated by Schroter, and this rejection should be withdrawn.

c.) Finally, the logic sequencer of Claim 1 causes the instruction pipeline to receive, and to initiate concurrent execution on, the predetermined number of the instructions in a ***predetermined period of time***. This aspect of Applicants' invention is described in Applicants' Specification as follows:

"By way of example, consider an instruction pipeline capable of initiating simultaneous execution on, at most, N instructions during N periods of the system clock where N is a positive integer. The current invention allows the pipeline execution to be controlled such that during every N clock periods, precisely N-1 instructions begin execution rather than the default number of N that is executed when the instruction processor is executing in the full-speed, default mode." (Applicants' Specification page 7 lines 9-14.)

Schroter does not describe any apparatus or method for controlling execution of any number of instructions in any *predetermined period of time*. In fact, Schroter does not appear to mention any particular time period associated with instruction execution, or any particular number of instructions that may be executed concurrently by the various execution units of the system. For this additional reason, Schroter does not anticipate, or even suggest, Applicants' system of Claim 1.

For at least the foregoing reasons, Schroter does not anticipate Applicants' Claim 1, and this rejection should be withdrawn.

Turning now to Claim 11, this method Claim includes aspects of Applicants' invention that are similar to those discussed above with respect to Claim 1. In particular, it describes utilizing a pipeline controller to cause the instruction pipeline to initiate execution of a number of instructions specified by a count within a predetermined period of time. For at least the reasons discussed above with regards to Claim 1, Schroter does not anticipate this Claim, and this rejection should be withdrawn.

Finally, apparatus Claim 19 includes aspects of Applicants' invention that are similar to those discussed above with respect to Claim 1. In particular, it describes sequencer means for controlling the entry of instructions into the instruction pipeline such that concurrent execution is initiated for a predetermined number of instruction within a predetermined period of time. For at least the reasons discussed above with regards to Claim 1, Schroter does not anticipate Claim 19, and this rejection should be withdrawn.

2. Applicants' Representative appreciatively acknowledges the indication of allowable subject matter in Claims 2-10, 12-18, and 20-22. It is respectfully submitted that in view of the reasons set forth above, these Claims are allowable as presently presented.

### CONCLUSION

Claims 1-22 were pending in the subject case. In the Office Action dated 10/24/02, Claims 1, 11, and 19 were rejected, and 2-10 and 12-18, and 20-22 were objected to. Claims 1-22 remain pending as previously presented. In view of the reasons set forth above, it is respectfully submitted the Claims are in condition for allowance. If the Examiner has questions or concerns regarding this response, a call to the undersigned is encouraged and welcomed.

Respectfully submitted,



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Beth L. McMahon  
Attorney for Applicants  
Reg. No. 41,987  
Tele No. (651) 635-7893

Unisys Corporation  
M.S. 4773  
P.O. Box 64942  
St. Paul, MN 55164-0942

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